IN THE CLAIMS:

1. (previously presented) A test method of a semiconductor integrated circuit device comprising:

providing the semiconductor integrated circuit device including a logic circuit, a supply voltage of the logic circuit for normal operation being a first voltage;

applying substrate bias voltages to MOS transistors of the logic circuit in order to enlarge threshold voltages of the MOS transistors;

applying a second voltage lower than the first voltage to the logic circuit as the supply voltage of the logic circuit; and

measuring a power supply current of the semiconductor integrated circuit device when the MOS transistors of the logic circuit are in stationary state.

2. (original) The test method of the semiconductor integrated circuit device according to claim 1, wherein the semiconductor integrated circuit device has a first pad capable of being applied with the substrate bias voltage and a second pad capable of being applied with the supply voltage.

3. (original) The test method of the semiconductor integrated circuit device according to claim 2, wherein the first pad is not connected to any pin of a package of the semiconductor integrated circuit device and the second pad is connected to one of pins of the package.

4. (original) The test method of the semiconductor integrated circuit device according to claim 1, further comprising:

selecting the semiconductor integrated circuit device as a confonning item when the measured power supply current is lower than a predetermined value.

5. (original) The test method of the semiconductor integrated circuit device according to claim 4, further comprising:

applying substrate bias voltages to MOS transistors of the logic circuit of the selected semiconductor integrated circuit device for normal operation;

applying the first voltage to the logic circuit of the selected semiconductor integrated circuit device as the supply voltage of the logic circuit; and

executing a function test for the selected semiconductor integrated circuit device.

6. (original) A test method of a semiconductor integrated circuit device comprising:

providing the semiconductor integrated circuit device including a logic circuit, a supply voltage of the logic circuit for normal operation being a first voltage and an absolute value of a threshold voltage of a MOS transistor of the logic circuit for normal operation being a second voltage; and

executing a first IDDQ test of the semiconductor integrated circuit device;

wherein, in the executing the first IDDQ test, the supply voltage is set to be a third voltage lower than the first voltage and the absolute value of the threshold voltage is set to be a fourth voltage higher than the second voltage.

7. (original) The test method of the semiconductor integrated circuit device according to claim 6, wherein a substrate bias voltage applied to the MOS transistor is controlled in order to control the threshold voltage of the MOS transistor.

8. (original) The test method of the semiconductor integrated circuit device according to claim 7, wherein the semiconductor integrated circuit device has a first pad capable of being applied with the substrate bias voltage and a second pad capable of being applied with the supply voltage.

9. (original) The test method of the semiconductor integrated circuit device according to claim 8, wherein the first pad is not connected to any pin of a package of the semiconductor integrated circuit device and the second pad is connected to one of pins of the package.

10. (original) The test method of the semiconductor integrated circuit device according to claim 6, further comprising:

applying a fifth voltage higher than the first voltage to the logic circuit as the supply voltage of the logic circuit before executing the first IDDQ test.

11. (original) The test method of the semiconductor integrated circuit device according to claim 6, further comprising:

selecting the semiconductor integrated circuit device as a conforming item when a measured power supply current in the executing the first IDDQ test is lower than a predetermined value.

12. (currently amended) The test method of the semiconductor integrated circuit device according to claim [[1]] 6, further comprising:

executing a second IDDQ test of the semiconductor integrated circuit device;

wherein, in the executing the second IDDQ test, the supply voltage is set to be the third voltage lower than the first voltage and the absolute value of the threshold voltage is set to be fourth voltage higher than the second voltage.

13. (original) The test method of the semiconductor integrated circuit device according to claim 12, further comprising:

selecting the semiconductor integrated circuit device as a conforming item based on a difference between a first measured power supply current in the executing the first IDDQ test and a second measured power supply current in the executing the second IDDQ test.

14. (original) The test method of the semiconductor integrated circuit device according to claim 11, further comprising:

executing a function test of the semiconductor integrated circuit device;

wherein, the executing the function test, the supply voltage is set to be the first voltage and the absolute value of the threshold voltage is set to be then the second voltage.